

Notice of Allowability

Application No.

10/813,152

Examiner

Ji H. Bae

Applicant(s)

KINSTLER, GARY A.

Art Unit

2115

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to amendments filed on 1-31-2007.
2. ☒ The allowed claim(s) is/are 2-11, 18, 19, 21, 22, 29, 30, 32-38.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some* c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
(a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
(b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|--|
| 1. <input type="checkbox"/> Notice of References Cited (PTO-892) | 5. <input type="checkbox"/> Notice of Informal Patent Application |
| 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 6. <input checked="" type="checkbox"/> Interview Summary (PTO-413),
Paper No./Mail Date <u>20070214</u> . |
| 3. <input type="checkbox"/> Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____ | 7. <input checked="" type="checkbox"/> Examiner's Amendment/Comment |
| 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 8. <input type="checkbox"/> Examiner's Statement of Reasons for Allowance |
| | 9. <input type="checkbox"/> Other _____. |

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Rustan J. Hill (No. 60483) on 14 February 14, 2007.

The application has been amended as follows:

In the claims:

Claim 2, amended to read:

A network interface apparatus comprising:

a bus interface circuit for operatively connecting a network interface card to a data bus, wherein the bus interface circuit is a physical layer controller;

a power controller operatively connected to the bus interface circuit;

a first current sensor operatively connected to the bus interface circuit to sense a first current level in the bus interface circuit; and

means for determining whether the first sensed current level exceeds a predetermined level and for causing the power controller to cycle power to the bus interface circuit in response to determining that the first sensed current level exceeds the predetermined level;

a link layer controller operatively connected to the data bus via the physical layer controller;

a second power controller operatively connected to the link layer controller; and

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a second current sensor operatively connected to the link layer controller to sense a second current level in the link layer controller;

wherein the means for determining and for causing further comprises means for determining whether the second sensed current level exceeds the predetermined level and for causing the power controller to cycle power to the physical layer controller and the second power controller to cycle power to the link layer controller in response to determining that one of the first sensed current level or the second sensed current level exceeds the predetermined level.

Claim 3, amended to read:

A network interface apparatus of claim 2, further comprising a switch operatively configured to select one of the first and second current sensors to report the selected sensed current level to the means for determining whether the selected sensed current level exceeds the predetermined level and for causing the power controller to cycle power to the bus interface circuit in response to determining that the selected sensed current level exceeds the predetermined level.

Claim 4, line 5, deleted "respective" before "sensed", inserted before "sensed", -- selected --.

Claim 6,

lines 1 and 2, deleted "further comprises a physical layer controller operatively connected between the bus interface circuit and the data bus";

line 3, deleted "the bus interface circuit is a link layer controller and" after "wherein".

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Claim 7,

lines 1-3, deleted "further comprises a link layer controller operatively connected to the data bus upstream from the bus interface circuit";

line 3, deleted "the bus interface circuit is a physical layer controller and" after "wherein".

Claim 11, amended to read:

A method in a data processing system including a network having a data bus, the method comprising:

sensing a current level in a bus interface circuit operatively connecting a node on the network to the data bus;

determining whether the sensed current level exceeds a predetermined level; and

re-initializing the bus interface circuit in response to determining that the sensed current level exceeds the predetermined level,

wherein the bus interface circuit is one of a plurality of bus interface circuits of the node operatively connecting the node to the data bus and sensing a current level comprises selecting the sensed current level associated with one of the plurality of bus interface circuits;

wherein a first one of the plurality of bus interface circuits is a physical layer controller;

wherein re-initializing the first one of the plurality of bus interface circuits comprises inhibiting a current from a power bus from reaching the physical layer controller; and

wherein a second of the plurality of bus interface circuits is a link layer controller and re-initializing the second of the plurality of bus interface circuits comprises inhibiting a current from the link layer controller from reaching the physical layer controller.

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Claim 18, amended to read:

A method of claim 11, further comprising providing a test signal to one of the plurality of bus interface circuits to cause the sensed current level to exceed the predetermined level.

Claim 19, amended to read:

A method of claim 11 wherein re-initializing one of the plurality of bus interface circuits is completed within a period equal to or greater than 10 milliseconds.

Claim 20, cancelled.

Claim 21, amended to read:

A method of claim 11, wherein the current levels in the first and second of the plurality of bus interface circuits are sensed substantially simultaneously.

Claim 22, amended to read:

A computer-readable medium containing instructions causing a program in a data processing system to perform a method, the data processing system including a network having a data bus, the method comprising:

sensing a current level in a bus interface circuit operatively connecting a node on the network to the data bus;

determining whether the sensed current level exceeds a predetermined level; and

re-initializing the bus interface circuit in response to determining that the sensed current level exceeds the predetermined level,

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wherein the bus interface circuit is one of a plurality of bus interface circuits of the node operatively connecting the node to the data bus and sensing a current level comprises selecting the sensed current level associated with one of the plurality of bus interface circuits;

wherein a first one of the plurality of bus interface circuits is a physical layer controller;

wherein re-initializing the first one of the plurality of bus interface circuits comprises inhibiting a current from a power bus from reaching the physical layer controller; and

wherein a second of the plurality of bus interface circuits is a link layer controller and re-initializing the second of the plurality of bus interface circuits comprises inhibiting a current from the link layer controller from reaching the physical layer controller.

Claim 29, amended to read:

A computer-readable medium of claim 22, further comprising providing a test signal to one of the plurality of bus interface circuits to cause the sensed current level to exceed the predetermined level.

Claim 30, amended to read:

A computer-readable medium of claim 22 wherein re-initializing one of the plurality of bus interface circuits is completed within a period equal to or greater than 10 milliseconds.

Claim 31, cancelled.

Claim 32, amended to read:

A computer-readable medium of claim 22, wherein the current levels in the first and second of the plurality of bus interface circuits are sensed substantially simultaneously.

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Claim 33,

line 2, inserted before "bus", second instance, -- first --;

line 4, inserted before "current sensor", -- first --;

line 4, inserted before "current level", -- first --;

line 6, inserted before "sensed current level", -- first --;

line 8, inserted before "sensed current level", -- first --.

Claim 34,

line 2, deleted "selectively allow" after "configured to", inserted after "configured to", --
select --;

line 3, deleted "respective" before "sensed current", inserted before "sensed current", --
selected --.

Claim 35,

line 3, deleted "another" before "bus", inserted before "bus", -- a second --;

line 6, deleted "respective" before "sensed current level", inserted before "sensed current
level", -- selected --;

line 6, deleted "other" before "bus", inserted before "bus", -- second --.

Claim 37,

lines 1 and 2, deleted "further comprises a physical layer controller operatively
connected between the bus interface circuit and the bus";

line 3, deleted "the bus interface circuit is a link layer controller and" after "wherein".

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Claim 38, lines 1-3, deleted "further comprising a link layer controller operatively connected to the bus upstream from the bus interface circuit";

line 3, deleted "the bus interface circuit is a physical layer controller" after "wherein".

Claim 39, cancelled.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ji H. Bae whose telephone number is 571-272-7181. The examiner can normally be reached on Monday-Friday, 10 am to 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ji H. Bae
Patent Examiner
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A handwritten signature in black ink, appearing to read 'Chun Cao', is positioned above the printed name.

CHUN CAO
PRIMARY EXAMINER